CATHODE PLATE OF A CARBON NANO TUBE FIELD EMISSION DISPLAY AND ITS FABRICATION METHOD

FIELD OF THE INVENTION

[0001] The present invention generally relates to a field emission display (FED), and more specifically to a cathode plate of a carbon nano tube (CNT) FED and its fabrication method.

BACKGROUND OF THE INVENTION

[0002] Although liquid crystal display (LCD) has become one of the most popular display devices, many researches on different kinds of display technologies are being pursued. One of them is the field emission display that has the potential to replace the conventional liquid crystal display in the display market. Unlike the conventional cathode ray tube (CRT) that uses a hot cathode electron gun, a field emission display uses cold cathode emitter tips as the electron source. When a field emission display is placed in an electric field, cold cathode emitter tips aim at the phosphor-coated anode substrate that is fabricated in the field emission display and emit a bundle of electrons.

[0003] FIG. 1 shows a schematic diagram of a conventional field emission display. Electrons, being attracted by an electric field and emitted out of the cold cathode 102 emitter tip 103 on the cathode glass substrate 101, are accelerated by the positive voltage applied to the anode substrate 104 to hit the coated phosphor 106 on the anode 105 and then produce luminescence.

[0004] Most conventional cathode plates of field emission displays are fabricated by

a screen printing method. In this method, a pre-mixed paste is applied to the surface of a pre-patterned screen and scraped using a scraper to print the pattern onto a substrate. Such process is repeatedly used to stack layers of patterns. The method has some drawbacks. It is difficult to increase the resolution of the printed pattern because of the limitation of the size of the screen mesh. The initial field emission voltage must be high enough to get sufficient brightness for the display. Also, the thickness of the printing film may not be uniform enough and the printed pattern may be inaccurate due to the non-uniform tension of the screen. Therefore, the distribution of the electric field is non-uniform and the alignment at post-process is difficult.

[0005] In order to be accepted in the display market, field emission displays must overcome the above-mentioned drawbacks by exploring a new fabrication method. The new fabrication method has to be capable of increasing the resolution of the printed pattern as well as the uniformity of the thickness of the printing film. It must also be able to arrange patterns arbitrarily to increase the function of the display.

SUMMARY OF THE INVENTION

[0006] This invention has been made to overcome the above-mentioned drawbacks of conventional field emission displays. The primary object is to provide a fabrication method for the cathode plate of a carbon nano tube field emission display. By combining photolithography process and etching process, the method uses a photoconductive paste and an etchable dielectric material to fabricate the cathode plate of a carbon nano tube field emission display.

[0007] According to this invention, the fabrication method for the cathode plate of a

carbon nano tube field emission display comprises the preparation of a transparent substrate and the fabrication of a cathode electrode layer, a dielectric layer, a gate layer, and a CNT emission layer. During the fabrication, a transparent substrate having top and bottom surfaces is first prepared. A layer of photoconductive paste is deposited on a surface of the transparent substrate. A pattern is then defined by a photolithography process and sintered to finish a cathode electrode layer.

[0008] The whole surface of the cathode electrode layer is deposited with a layer of etchable dielectric material. A layer of photoconductive gate material is further deposited on the dielectric layer. Gate patterns are then printed by a photolithography process and sintered to finish a gate electrode layer. The gate pattern is used as a protecting film to etch a portion of the dielectric layer not covered by the protecting film in a photolithography process and finally a CNT emission layer is filled on the cathode electrode layer to form a cathode plate structure.

[0009] In the preferred embodiments of this invention, the transparent substrate, such as a glass substrate, has top and bottom surfaces. The photolithography process includes the definition of a pattern by a photo-mask after pre-bake, photo exposure and development. Before filling the CNT emission layer, the gate pattern is used as a protecting film to etch a portion of the dielectric layer to form a dielectric pattern in a photolithography process. The CNT emission layer can be filled by a photolithography method or an electrical deposition method. In the present invention, following the fabrication of the cathode electrode layer, the CNT emission layer can also be fabricated before the dielectric layer and the gate electrode layer by a screen printing method.

[0010] According to this invention, the cathode plate in a carbon nano tube field

emission display can increase the resolution of patterns as well as the uniformity of the film thickness. Also, patterns can be arbitrarily arranged. Packing this cathode plate structure and a conventional anode plate together can make a CNT field emission array.

[0011] In a preferred embodiment of the invention, the line width of the CNT field emission array can be as small as 30 μm per line space in a photolithography process under the conditions that the exposure energy for the photolithography process is 300-500 mJ, the development is at 20-25 °C room temperature, and the weight percentage (wt%) of the K_2CO_3 solution is 0.5-0.7. Comparing with patterns fabricated by conventional screen printing methods, the resolution of the printed pattern is significantly increased by this invention. The resolution of the dielectric layer can be decided during the fabrication process for the gate electrode layer. This reduces the complicated alignment and simplifies the fabrication process. Therefore, the quality of the display is improved.

[0012] The foregoing and other objects, features, aspects and advantages of the present invention will become better understood from a careful reading of a detailed description provided herein below with appropriate reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. 1 shows a schematic diagram of a conventional field emission display.

[0014] FIG. 2a shows a perspective view of a cathode plate of a carbon nano tube field emission display according to this invention.

[0015] FIG. 2b shows a top view of a conventional anode plate of a field emission display.

[0016] FIG. 3 illustrates the fabrication process for the cathode electrode layer of a cathode plate according to a first embodiment of the invention.

[0017] FIG. 4 illustrates the fabrication process for the dielectric layer of a cathode plate according to a first embodiment of the invention.

[0018] FIG. 5 illustrates the fabrication process for the gate electrode layer of a cathode plate according to a first embodiment of the invention.

[0019] FIG. 6 illustrates the fabrication process for the CNT emission layer of a cathode plate according to a first embodiment of the invention.

[0020] FIGs. 7-10 illustrate the fabrication process for the CNT emission layer, the dielectric layer, and the gate electrode layer of a cathode plate in a carbon nano tube field emission display after the fabrication of a cathode electrode layer as shown in FIG. 3b according to another embodiment of the invention.

[0021] FIG. 11 shows an enlarged picture of the cathode electrode layer and the gate electrode layer of a cathode plate according to the invention.

[0022] FIG. 12 shows an enlarged picture of cathode electrode patterns fabricated by a conventional screen printing method as well as by a photolithography method of this invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0023] FIG. 2a shows a perspective view of the cathode plate of a carbon nano tube field emission display according to this invention. Referring to FIG. 2a, the cathode plate comprises a transparent substrate 201, a cathode electrode layer 203, a dielectric layer

205, a gate electrode layer 207, and a CNT emission layer 209 that are arranged in order from the bottom to the top. The cathode electrode layer 203 comprises multiple parallel electrode strips. The dielectric layer 205 comprises multiple parallel strips of dielectric material. The gate electrode layer 207 comprises multiple parallel electrode strips. Each gate electrode strip is located on the top of a dielectric strip and is perpendicular to cathode electrode strips. There are circular holes on gate electrode strips and dielectric strips at intersections with cathode electrode strips. The circular holes are the field emission regions where the CNT emission layer 209 is filled therein.

[0024] According to the invention, the dielectric layer can be composed of a surface film. However, the process needs an extra photolithography process to make the circular holes at every intersection between gate electrode strips and cathode electrode strips.

[0025] In a preferred embodiment of this invention, the width of a cathode electrode strip or a dielectric strip is in the range of 30 μm to 300 μm and the gap between two parallel strips is in the range of 30 μm to 50 μm. The diameter of each circular hole, as shown in FIG 2a, can be 10 μm to 50 μm. The thickness of the cathode electrode layer is in the range of 3.5 μm to 5.5 μm. The thickness of the dielectric layer is in the range of 10 μm to 30 μm. The thickness of the gate layer is in the range of 3.5 μm to 5.5 μm. The thickness of the CNT emission layer is in the range of 3 μm to 5 μm.

[0026] A CNT field emission array is made by combining this cathode plate structure with a conventional anode plate of a field emission display and packing them together. FIG. 2b shows a top view of a conventional anode plate of a field emission display. The anode plate comprises a panel 211, a transparent electrode layer 213 and a layer of

fluorescent material 215.

[0027] With reference to FIGs. 3-6, the following describes in detail, with a preferred embodiment, the fabrication process for the cathode electrode layer, the dielectric layer, the gate electrode layer, and the CNT emission layer of the cathode plate in a carbon nano tube field emission display shown in. FIG. 2a. FIG. 3 illustrates the fabrication process for the cathode electrode layer of the cathode plate according to the invention.

[0028] Referring to FIG. 3a, the fabrication process of the cathode electrode layer comprises the steps or preparing a transparent substrate 201 having top and bottom surfaces, depositing a layer of photoconductive paste 301 on a surface of the transparent substrate 201, defining a pattern by photolithography process and sintering to form a cathode electrode layer 203. The photolithography process includes the definition of a pattern by a photo-mask 303 after pre-bake, and the steps of photo exposure 305 and development. FIG. 3b illustrates a cross sectional view of a pattern of the cathode electrode layer 203 after developing.

[0029] In the preferred embodiments of the present invention, the photoconductive paste can be made by mixing conductive metal powder and resin with solvent and photosensitive emulsion. The conductive metal powder can be silver (Ag), nickel (Ni), or chromium (Cr). The resin can be trimethylpentanediol monoisobutyrate, acrylic resin, or methyl acrylate. The sintering time is about 30 minutes at a temperature between 480 °C to 560 °C in an air atmosphere. The transparent substrate is usually a glass substrate.

[0030] After the cathode electrode layer 203 is fabricated, a layer of etchable dielectric material is deposited on the whole surface of the cathode electrode layer 203 and the substrate. The cross sectional view of the dielectric layer 205 is shown in FIG. 4.

In the preferred embodiments of the present invention, the dielectric material can be formed by mixing dielectric powder and resin with solvent. The dielectric powder can be SiO_2, Na_2O, Li_2O, PbO_2 or BO_2. The resin can be trimethylpentanediol monoisobutyrate, acrylic resin, or methyl acrylate.

[0031] FIG. 5 illustrates the fabrication process for the gate electrode layer of the cathode plate in a carbon nano tube field emission display according to the invention. A layer of photoconductive gate material 501 is deposited on the whole surface of the dielectric layer 205. After photolithography process and sintering, a gate pattern 207 is formed. In this embodiment, the dielectric layer is sintered to burn away the residual organic material in each layer before depositing the layer of photoconductive gate material 501. The sintering time is about 30 minutes at a temperature between 480 °C to 540 °C in an air atmosphere. The photolithography process includes defining a pattern by a photo-mask 503 after pre-bake, photo exposure 505 and developing. FIG. 5b illustrates a cross sectional view of a pattern of the gate electrode layer 207 after the development.

[0032] In the preferred embodiments of the present invention, the material, the sintering time and the temperature used for the gate electrode layer are the same as those used for the cathode electrode layer. The deposition method includes spin, roller and screen-printing. The solvent for all layers mentioned-above can be the combination of carboxylic acid, aliphatic acid, ethyl 4-dimethylaminobenzoate, and 2,2-dimethoxy-2-phenyl acetophenone. The solid content of the paste is about 50-65%.

[0033] FIG. 6 illustrates the fabrication process for the CNT emission layer of the cathode plate in a carbon nano tube field emission display according to the invention. The gate pattern 207 is used as a protecting film to etch a portion of the dielectric layer not

covered by the protecting film in a photolithography process. Finally, the CNT emission layer 209 is deposited on the cathode electrode layer 203 to form a cathode plate structure. In this embodiment, the etching process etches the dielectric layer 205 to form a dielectric pattern 601. The residual organic material in each layer is burn away by sintering. The cross sectional view of the structure after sintering is shown in FIG. 6a.

[0034] According to this invention, the CNT emission layer 209 can be fabricated on the cathode electrode layer 203 by a photolithography method or an electrical deposition method. FIG. 6b illustrates a cross sectional view of a complete cathode plate structure. The following describes these two methods in more detail.

[0035] The fabrication of the CNT emission layer using a photolithography method is accomplished by depositing a layer of photosensitive CNT paste on the surface of the cathode plate shown in FIG. 6a and define a pattern for the CNT emission layer as shown in FIG. 6b by alignment and exposure. It is then sintered for 30 minutes in a 480 °C to 500 °C oven in an nitrogen atmosphere. The photosensitive CNT paste can be made by mixing positive or negative photoresist with CNT powder of 5-30 weight percentage and silver (Ag) powder of 5-30 weight percentage.

[0036] The fabrication of the CNT emission layer using an electrical deposition method comprises the steps of depositing a layer of positive or negative photoresist on the surface of the cathode electrode layer 203 and the gate electrode layer 207 shown in FIG. 6a, and using a mask to define a photoresist pattern by alignment and exposure. After the photoresist pattern is formed above the gate pattern 207, the CNT emission layer is then formed by electrically depositing a CNT paste into the field emission region on the cathode electrode pattern 203 for 30-60 seconds at 35 volts, and sintering for 30

minutes in a 480 °C to 500 °C oven at a nitrogen atmosphere.

[0037] The CNT paste for the electrical deposition method can be made by mixing CNT powder of 3-50 weight percentage and water (H_2O) with a dispersant, such as carboxyl methyl cellulose (CMC) of 0.02-0.2 grams per liter.

[0038] In addition to the fabrication process shown in FIGs. 3-6, the following describes the fabrication process for a cathode plate of the invention with another preferred embodiment. The fabrication process comprises the preparation of a transparent substrate and the fabrication of the cathode electrode layer, the CNT emission layer, the dielectric layer, and the gate electrode layer in sequence. In other words, following the fabrication of the cathode electrode layer shown in FIG. 3b, the CNT emission layer is fabricated before the dielectric layer and the gate electrode layer, as shown in FIGs. 7-10.

[0039] After the fabrication of the cathode electrode layer 203 shown in FIG. 3b, a CNT emission layer 209 is printed on the pattern of the cathode electrode layer 203 by a screen printing method, as shown in FIG. 7. Then a layer of etchable dielectric material is deposited on the whole surface of the device as a dielectric layer 205, as shown in FIG. 8. The fabrication process for the gate electrode layer shown in FIGs. 9a-9b is the same as that shown in FIGs. 5a-5b. After developing the gate electrode layer 207 shown in FIG. 9b, the gate pattern 207 is used as a protecting film to etch a dielectric layer 205 and form a dielectric pattern 601. Then the residual organic material in each layer is burn away and the cathode plate structure is completed, as shown in FIG. 10.

[0040] The resolution of the dielectric layer can be decided during the fabrication process for the gate electrode layer. Accordingly, this invention reduces the complicated alignment and simplifies the fabrication process. It also increases the resolution of

patterns as well as the uniformity of the film thickness. Patterns can be arbitrarily arranged too.

[0041] FIG. 11 shows an enlarged picture of the cathode electrode layer and the gate electrode layer of the cathode plate in a carbon nano tube field emission display according to the invention. Referring to FIG. 11, the horizontal strips are the cathode electrode patterns 1101, the vertical strips are the gate electrode patterns 1103, and the CNT emission layer 1105 is filled inside the circular holes of diameter 50 μm. The dielectric layer (not shown) is under the gate electrode patterns 1103. The CNT emission layer 1105 is filled by a photolithography method. The line width of the CNT field emission array can be as small as 30 μm per line space in a photolithography process under the conditions that the exposure energy for the photolithography process is 300-500 mJ, the development is at 20-25 °C room temperature, and the weight percentage of the K_2CO_3 solution is 0.5-0.7.

[0042] FIG. 12 shows an enlarged picture of cathode electrode patterns fabricated by a conventional screen printing method as well as by the photolithography method of this invention. Referring to FIG. 12, the strip width of the cathode electrode patterns 1201 (horizontal coarse lines) fabricated by a conventional screen printing method is greater than 100 μm. The strip width of the cathode electrode patterns 1203 (vertical thin lines) fabricated by the photolithography method of this invention is about 30 μm. As shown in FIG. 12, the resolution of the printed pattern is significantly increased by this invention. Therefore, the quality of the display is improved.

[0043] In summary, this invention uses photoconductive paste and etchable dielectric material and combines photolithography process and etching process to fabricate the

cathode plate of a carbon nano tube field emission display. It overcomes the drawback of conventional screen printing methods in which the resolution of the printed pattern is difficult to increase. The advantages of this invention also include simple fabrication process, uniform thickness of the film, and accurate printed patterns. Also, the distribution of the electric field is uniform and the alignment at the post-process is not difficult.

[0044] Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.